

ABSTRACT OF THE DISCLOSURE

Sort operations of an input signal are performed by providing a first sort part 6 comprising one shift circuit 8 and $(l-1)$ sort circuits 9a to 9c, and a second sort part 7 comprising one delay circuit 10, $(m-1)$ sort circuits 11a to 11c and m shift circuits 12a to 12d in a pattern synchronous circuit 100.

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